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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,025	10/16/2003	Kai Fechner	(H) 02PH0443USP	2169

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EXAMINER	
ANDREWS, LEON T	
ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/688,025	FECHNER ET AL.	
	Examiner	Art Unit	
	Leon Andrews	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/16/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Nelson et al. (Patent Number: 6,138185).

Regarding Claim 1, Nelson et al. discloses an interface module (Fig. 2, 200) (2a, 2b, 2c, 2d) comprising:

a first number of a series (Fig. 2, 201) (5a, 5b, 5c, 5d) of ports (51a, 52a, 53a, 54a, 51b, 51c, 51d) (Fig. 2, 201a, 201b...201f..) and

a second number of a series (Fig. 2, 201) (6a, 6b, 6c, 6d) of ports (61a, 62a, 63a, 64a) (Fig. 2, 201c, 201d...), where a first port (51a, 51b, 51c, 51d) (Fig. 2, 201a) in the first number of a series of ports (51a, 52a, 53a, 54a, 51b, 51c, 51d) (Fig. 2, 201a, 201b, 201e...201f..) is connected by means of at least one data line (Fig. 2, 209) to a switching control unit (3a, 3b, 3c,

3d) (Fig. 2, 203) connected to an interface device (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d), and where

the subsequent input ports (Fig. 2, 210b...201f..) (52a, 53a, 54a) in the first number of a series (Fig. 2, 201) (5a, 5b, 5c, 5d) of ports are connected in order by means of at least one respective data line (Fig. 2, 209) to the ports (Fig. 2, 201c, 201d...) (61a, 62a, 63a, 64a) in the series of the second number of a series (6a, 6b, 6c, 6d) of ports, starting with a first (Fig. 2, 201c) (61a) in the series of the second number of ports.

(Fig. 2, each port 201, labeled P, is an input/output (I/O) port that supports bi-directional data communication and contains transmit and receive circuitry; also, switch 200 could be configured with a plurality of dedicated input and output ports, column 3, lines 39-46).

Regarding Claim 2, Nelson et al. discloses the interface module as claimed in claim 1,

where the interface device comprises a number of Ethernet interfaces (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d, 11).

Regarding Claim 3, Nelson et al. discloses the interface module as claimed in claim 1,

where a specification (106 includes an expansion port, 107 includes fabric loop port, 109 includes node loop port, column 3, lines 23-30) of the interfaces of the interface device (4a, 4b, 4c, 4d) is taken place by means of at least interface utilisation module (Fig. 1, 101, 109) (20) which has to be connected to the interface device.

Regarding Claim 4, Nelson et al. discloses the interface module as claimed in claim 1,

where data lines are in the form of separate and multipole bus lines (Fig. 2, 205, 207, 209) (B1, B2, B3, B4).

Regarding Claim 5, Nelson et al. discloses an Ethernet switch (Fig. 2, 106, 107) comprising

a header device (Fig. 3, SCC 203) (1) with a crossbar device (Fig. 3, 302) (7) and a number of downstream interface modules (Fig. 2, 200) (2a, 2b, 2c, 2d), particularly a number of downstream interface modules, having a first number of a series (Fig. 2, 201) (5a, 5b, 5c, 5d) of ports and a second number of a series (Fig. 2, 201) (6a, 6b, 6c, 6d) of ports, respectively, such that in each case the same one (Fig. 2, 201a) (51a, 51b, 51c, 51d) in the series of the first number (5a, 5b, 5c, 5d) of ports is connected to a switching control unit (Fig. 2, 203) (3a, 3b, 3c, 3d) coupled to an interface device (Fig. 1, 111, 112, 113) (4a, 4b, 4c 4d), and the further ports (Fig. 2, 210b...201f..) (52a, 53a, 54a) in the series of the first number (5a, 5b, 5c, 5d) of ports are connected to a port in the second number (Fig. 2, 201) (6a, 6b, 6c, 6d) of the series of ports (Fig. 2, 201c, 201d...) by means of respective data lines (Fig. 2, 209) routed in cascade form.

Regarding Claim 6, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the crossbar device (7) comprises a multiplicity of bus lines (Fig. 2, 205, 207, 209) (B1, B2, B3, B4) which can be connected in a star-shaped form (Fig. 3) to respective switching control units (Fig. 2, 203) (3a, 3b, 3c, 3d).

Regarding Claim 7, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the header device (1) comprises an interface device (Fig. 1, 109) (11) which is connected to the crossbar device (7) by means of a bus line (Fig. 2, 209) directly or via a switching control unit (Fig. 2, 203) (9) in the header device (1).

Regarding Claim 8, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the interface device comprises a number of Ethernet interfaces (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d, 11).

Regarding Claim 9, Nelson et al. discloses the Ethernet switch as claimed in claim 5, comprising

at least one interface utilization module (Fig. 1, 101, 109) (20) connected to at least one interface device (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d, 11) for the specification of at least one interface (Fig. 1, 111) (44a).

Regarding Claim 10, Nelson et al. discloses the Ethernet switch as claimed in claim 9,

where the interface utilization module (20) is constructed as being an active module (Fig. 1; hub 109 {active} includes node loop ports supporting links to loop server 110, workstations 112, 113 and switch 107, column 3, lines 30-33), a passive module and/or a (buffer) memory module (Fig. 1; server 101 is a node device that stores node ports information, column 3, lines 6-7; Fig. 1, 104).

Regarding Claim 11, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the data lines (B1, B2, B3, B4) are each in the form of separate, multipole G.Link connections (Fig. 2, 205, 207, 209).

Regarding Claim 12, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the crossbar device (7) comprises a PCI interface (Fig. 3, 307) for connecting a management function device (Fig. 3, SCC 203 includes additional logic, memory and signal processing devices for performing any number of conventional port management functions, column 4, lines 40-42) (8).

Regarding Claim 13, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the design of the Ethernet switch is modular and/or extendable (Fig. 1, fabric ports are located in fabric devices such as switch 106 and switch 107, column 3, lines 8-9).

Regarding Claim 14, Nelson et al. discloses the Ethernet switch as claimed in claim 5,

where the bus lines (B1, B2, B3, B4) are arranged serially (plurality of serial request busses are arranged with its associated port, column 2, lines 30-32).

Regarding Claim 15, Nelson et al. discloses a method (method, column 3, line 67) for providing a multiplicity of switchable Ethernet terminals (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d), where a crossbar device (Fig. 3, 302) (7) (7) is connected to a multiplicity of separate multipole data lines (Fig. 2, 205, 207, 209) (B1, B2, B3, B4) having switching control units (Fig. 2, 203) (3a, 3b, 3c, 3d), which can be lined up in modular fashion and are associated with respective Ethernet

terminals (Fig. 1, 111, 112, 113) (4a, 4b, 4c, 4d), by means of a respective predefined data line (Fig. 2, 209) (B1, B2, B3, B4).

Regarding Claim 16, Nelson et al. discloses the method as claimed in claim 15,

in which each switching control unit (Fig. 2, 203) (3a, 3b, 3c, 3d) is produced as part of an interface module (Fig. 2, 200) (2a, 2b, 2c, 2d) such that information to be transmitted to a downstream interface module (Fig. 2, 200) (2b, 2c, 2d) from the crossbar device (7) is routed through the respective upstream interface module (2a, 2b, 2c) in cascade form (requests handled concurrently without being blocked, column 4, lines 8-11).

Regarding Claim 17, Nelson et al. discloses the method as claimed in claim 15,

where the determination of the plurality of switchable Ethernet terminals (4a, 4b, 4c, 4d) is taken place by connecting interface utilisation modules (Fig. 1, 101, 109) (20) thereto.

Citation of Pertinent Prior Art

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

DiGiorgio et al. (Patent No.: US 6,286,060 B1) discloses method and apparatus for providing modular I/O expansion of computing devices.

Szczepanek et al. (Patent No.: US 6,690,668 B1) discloses modular interconnection of network switches.

Dubreuil (Patent No.: US 6,804,193 B1) discloses protected Ethernet backplane communication.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Andrews whose telephone number is (571) 270-1801. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rao S. Seema can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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June 26, 2007